The Invention Claimed Is

1. A programmable logic device, comprising:

a first row of programmable logic regions;

a second row of programmable logic regions that is parallel to and immediately adjacent to the first row of logic regions;

a first conductor associated with each logic region of the first row that extends to the second row of logic regions, the first conductor being a conduit for which logic region output signals provided by the logic regions of the first row are applied substantially directly to the logic regions of the second row;

a second conductor associated with each of the logic regions in the first and second rows and extending from the associated logic region adjacent a first subplurality of others of the logic regions in the respective first and second rows that are adjacent to the associated logic region on a first side of the associated logic region;

a third conductor associated with each of the logic regions in the first and second rows and extending from the associated logic region adjacent a second subplurality of still others of the logic regions in the respective first and second rows that are adjacent to the associated logic region on a second side of the associated logic region; and

first programmable logic connector circuitry associated with each of the logic regions in the second row and operative to selectively apply the logic region output signal of a logic region of the first row or the logic region output signal of the associated logic

region to either or both of the first and second conductors associated with that logic region.

2. The device defined in claim 1 further comprising:

second programmable logic connector circuitry associated with at least some of the logic regions that each of the first and second conductors is adjacent to and operative to selectively apply a signal on that first or second conductor to the associated logic regions as a logic region input signal.

3. The device defined in claim 1 wherein the first programmable logic connector circuitry provides flexible clustering of logic regions by selectively routing logic region output signals among the logic regions forming the cluster via the first, second, and third conductors.

4. The device defined in claim 1 wherein the logic region output signal applied to the first conductor is applied to programmable logic connector circuitry associated with the logic region in the second row as logic region input signal.

5. The device defined in claim 1 further comprising:

a fourth conductor associated with each logic region of the second row that extends to the first row of logic regions, the second conductor being a conduit for which logic region output signals provided by the logic regions of the second row are applied

substantially directly to the logic regions of the first row.

6. The device defined in claim 5 further comprising:

third programmable logic connector circuitry associated with each of the logic regions in the first row and operative to selectively apply the logic region output signal of a logic region of the second row or the logic region output signal of the associated logic region to either or both of the first and second conductors associated with that logic region.

7. The device defined in claim 6, wherein the first and third programmable logic connector circuitry provides flexible clustering of logic regions by selectively routing logic region output signals among the logic regions forming the cluster via the first, second, third, and fourth conductors.

8. The PLD defined in claim 1, wherein each of the first subpluralities includes approximately a same first number of the logic regions.

9. The PLD defined in claim 1, wherein each of the second subpluralities
includes approximately a same number of the logic regions.

10. The PLD defined in claim 1, wherein the logic regions in the first and second rows are substantially aligned perpendicular to each other such that a particular logic region in the first row is in

the same column as a corresponding logic region in the second row.

11. A digital processing system comprising:

processing circuitry;

a memory coupled to said processing circuitry; and

a programmable logic integrated circuit device as defined in claim 1 coupled to the processing circuitry and the memory.

12. A printed circuit board on which is mounted a programmable logic integrated circuit device as defined in claim 1.

13. The printed circuit board defined in claim 12 further comprising:

a memory mounted on the printed circuit board and coupled to the programmable logic integrated circuit device.

14. The printed circuit board defined in claim 12 further comprising:

processing circuitry mounted on the printed circuit board and coupled to the programmable logic integrated circuit device.